LABORATORY NO. 5

A SIMPLE CPU

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CompE 324

Instructor:
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P R E L I M I N A R Y

Objectives:

The objective of this lab is to integrate a control unit into the previous Lab 4 exercise where the data path was created and the concrete RTN was developed. The control unit is a Moore state machine with input forming logic (IFL), a flip flop (FF), and output forming logic (OFL). The present state bits are fed back into the IFL to form the next state bits. The external memory will hold the set of instructions that will be referred to as "the program". This will inform the CPU what to do.

Procedures:

1. Using what was designed in Lab 4 and the SCPU handout, integrate a control unit into the data path.
    1. Determine the different stages of each instruction.
    2. Develop the present state and next state bits based off of the op code.
    3. Develop the outputs based on the present state.
        - The outputs are all of the control bits that go through the CPU and turn the different components on or off.
    4. Program the IFL and OFL
    5. Program the external memory to complete the steps necessary.

L A B O R A T O R Y W O R K

At the end of this laboratory, the full SCPU will be completed. You will be able to program the external memory and have the CPU complete the desired code.

Equipment Needed:

- *For the control unit:*
  - *1 1KRAM*
  - *2 PROM*
  - *1 74LS374 FF*

This section will consist of completed tables from the laboratory exercise as well as any Q&A problems.

IFL											OUTPUTS																PS	INS
OPER			P.S.				N.S.				ALU					AC		PC			DR		IR	AB	AR			
											M	3	2	1	0	E	B	J	INC	R	E	W?	E	CB	E		
x	x	x	0	0	0	0	0	0	0	1	x	x	x	x	x	0	0	0	0	0	0	x	0	1	1	0	F0
x	x	x	0	0	0	1	0	0	1	0	x	x	x	x	x	0	0	0	1	0	1	0	0	0	0	1	F1
0	1	0	0	0	1	0	0	0	1	1	x	x	x	x	x	0	0	0	0	0	0	x	1	0	0	2	F2
1	0	1	0	0	1	0	0	0	1	1	x	x	x	x	x	0	0	0	0	0	0	x	0	0	0	3	LD0
1	1	0	0	0	1	0	0	0	1	1	x	x	x	x	x	0	0	0	0	0	1	0	0	0	0	4	LD1
x	x	x	0	0	1	1	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	x	0	0	0	5	LD2
0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	1	1	0	0	0	0	0	x	0	0	0	6	ADD
1	0	1	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0	0	0	0	0	x	0	0	0	7	AND
1	1	0	0	1	0	0	0	1	1	0	x	x	x	x	x	0	0	1	0	0	0	x	0	0	0	8	JMP
0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	x	0	0	0	9	NOT
1	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	1	0	0	0	0	0	x	0	0	0	10	SHL
1	1	1	0	0	1	0	1	0	1	0	x	x	x	x	x	1	1	0	0	0	1	0	0	0	1	11	STO
0	1	1	0	0	1	0	1	0	1	1	x	x	x	x	x	0	0	0	0	0	1	1	0	0	0	12	ST1
x	x	x	1	0	1	1	1	1	0	0																	
x	x	x	0	1	1	1	0	0	0	0																	
x	x	x	0	1	1	0	0	0	0	0																	
x	x	x	0	1	0	1	0	0	0	0																	
x	x	x	1	0	0	0	0	0	0	0																	
x	x	x	1	0	0	1	0	0	0	0																	
x	x	x	1	0	1	0	0	0	0	0																	
x	x	x	1	1	0	0	0	0	0	0																	

Illustration 1: The IFL is on the left with the OFL on the right. Constructed by using the concrete RTN developed in the Lab 4.

Questions/Comments:

There are no questions or comments that need to be addressed.

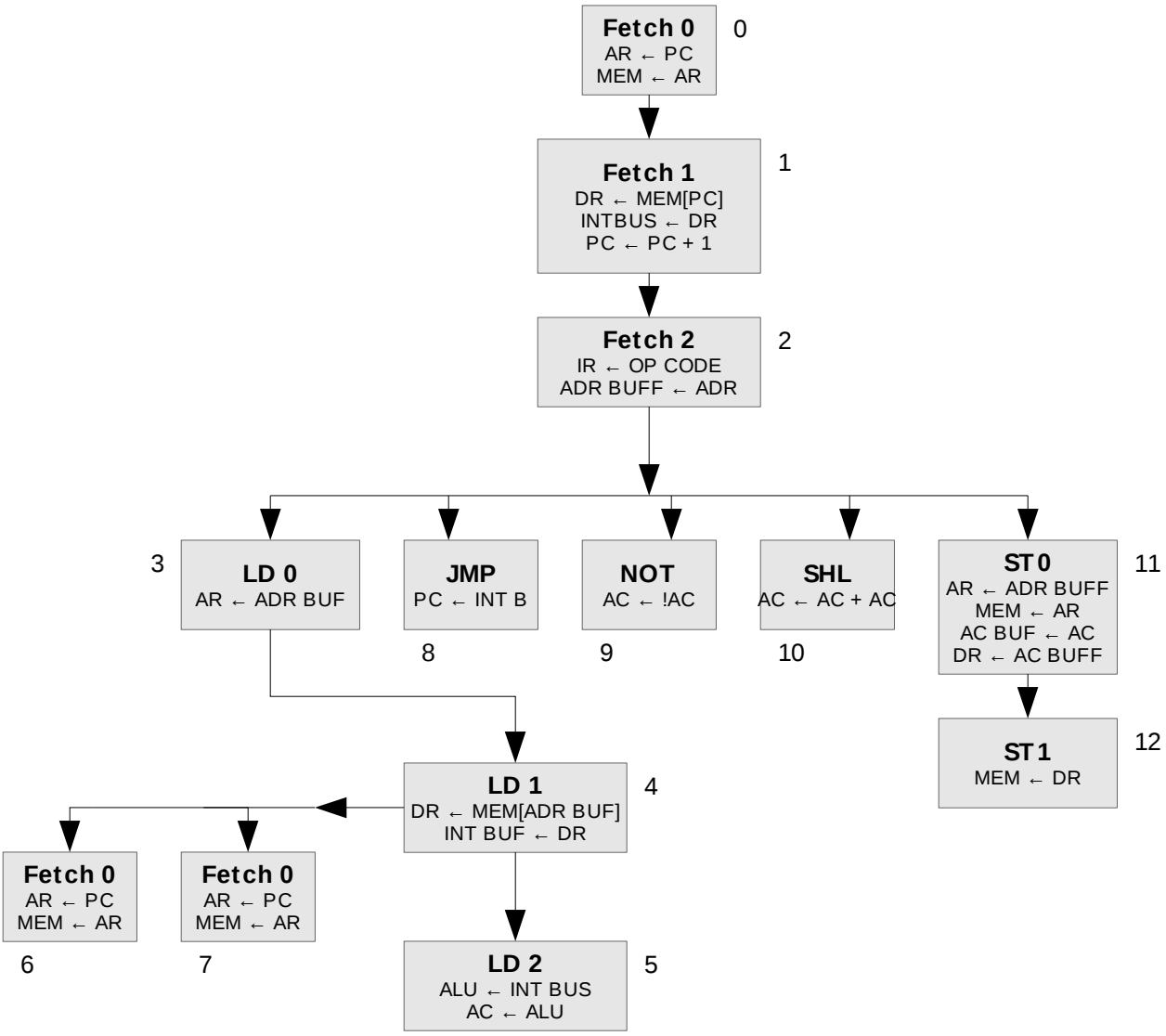
(CONT.) This section will consist of completed tables from the laboratory exercise.

IFL	
0 to 7	0 1
8 to 15	0 2
18	0 3
21	0 3
22	0 3
24 to 31	0 4
34	0 5
37	0 7
38	0 6
17	0 8
20	0 9
23	0 A
19	0 B
88 to 95	0 C

OFL		
PS	MSB	LSB
0	0 0	0 6
1	0 0	A 0
2	0 0	0 8
3	0 0	0 0
4	0 0	0 0
5	D 4	2 0
6	4 C	0 0
7	D C	0 0
8	0 1	0 0
9	8 4	0 0
10	6 4	0 0
11	0 6	2 2
12	0 0	3 0

Illustration 2: Quick cheat cheet to program the IFL and OFL.

This section will consist of the flow chart that was used to complete the lab.



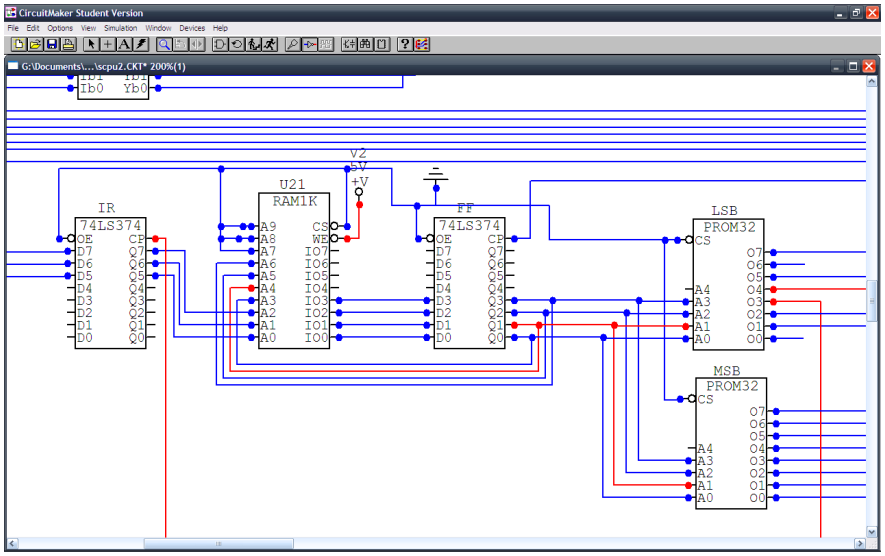


Illustration 3: The control unit

This section will consist of other drawings that were used to complete the lab.

This section will consist of the overall schematics that were used to complete the lab.

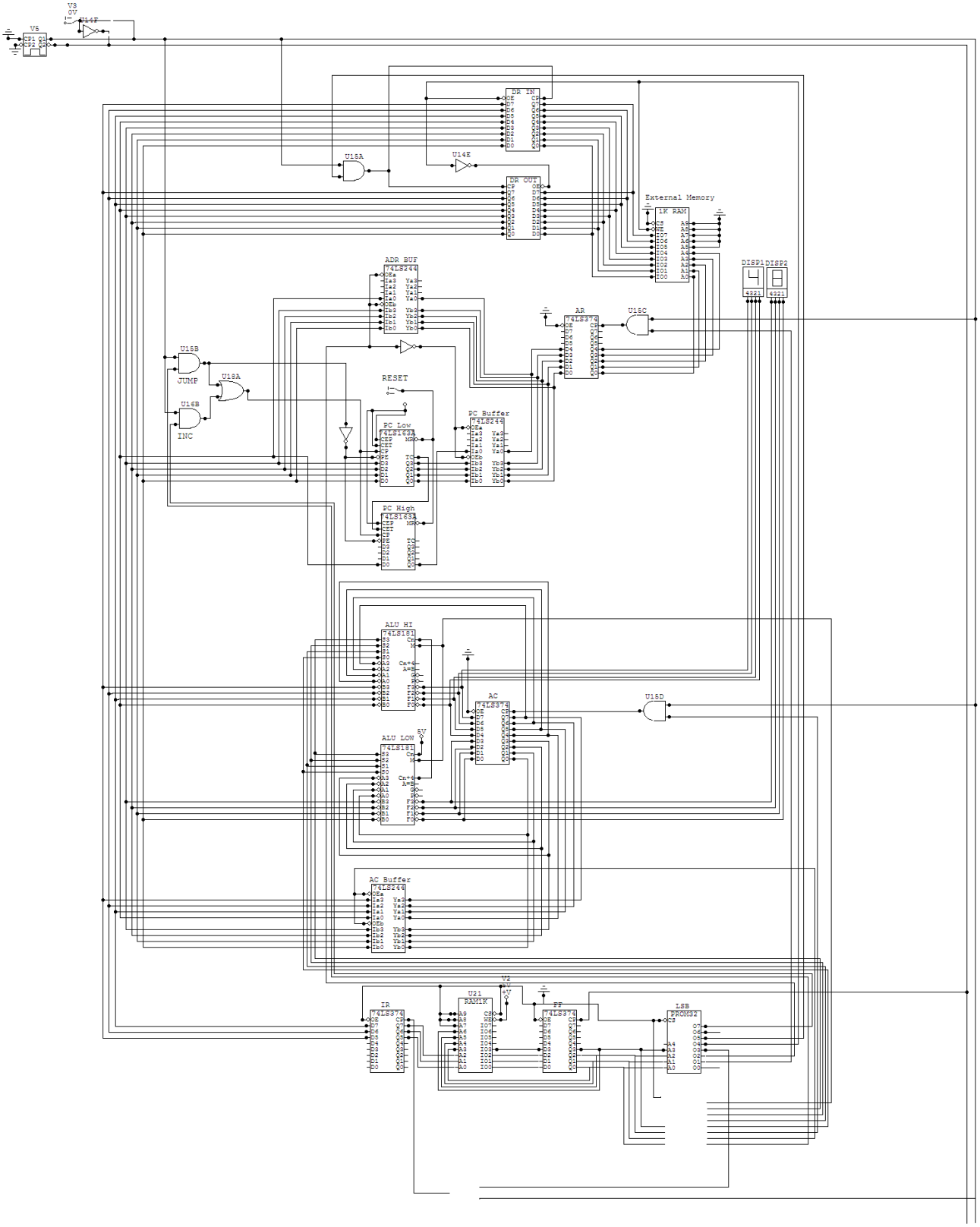


Illustration 4: The overall scheme for the SCPU. Notice the 2nd ROM of the control unit is missing. This is a flaw in circuit maker.

C O N C L U S I O N

This laboratory was interesting because there was no formal lab instructions that the students had to follow like in the other labs. What was given was a handout by the teacher (the same one in Lab 4) that outlined what all of the different commands were going to be for the control unit. The concrete RTN was developed by the classmates and applied to this lab.

It's amazing how complicated and difficult designing a control unit can become. Even after the IFL and OFL with outputs was completed, there was still much to debate on how the overall SCPU was going to function. We were briefed by the instructor in class and got a good start into the design, but it was still difficult getting everything up and functional. One disappointing piece of the lab was that we couldn't figure out how to use PROMs for the IFL. We were able to get a 1KRAM to work, although we have to re-program it every time we shut down circuit maker. Also, it would've been nice to keep a designated program for the external memory as well. Given more time, this would have been pretty simple to implement with a counter and PROMs.

It's hard to narrow down a specific few “kinks”, or things that we had a hard time with, in this lab because everything seemed to go wrong. The external memory and the data registers along with the accumulator were among the difficult things to fix. One problem was linked to a timing delay found in a not gate connecting the data registers together. This was fixed with a quick hack to the IFL and re-positioning the gate. Another was the program counter. Plans changed right at the end of the design and so some hacks were deployed to get it working properly. Because of the unexpected change, there was a lot of unexpected time that had to go into the program counter.

In the end, it was very neat to have a full, working simple CPU that we were able to program and tell it what to do. It makes me appreciate what goes into modern CPU architecture a lot more and I'm anxious to learn more about it.